

Figure 1

Figure 2

DEF

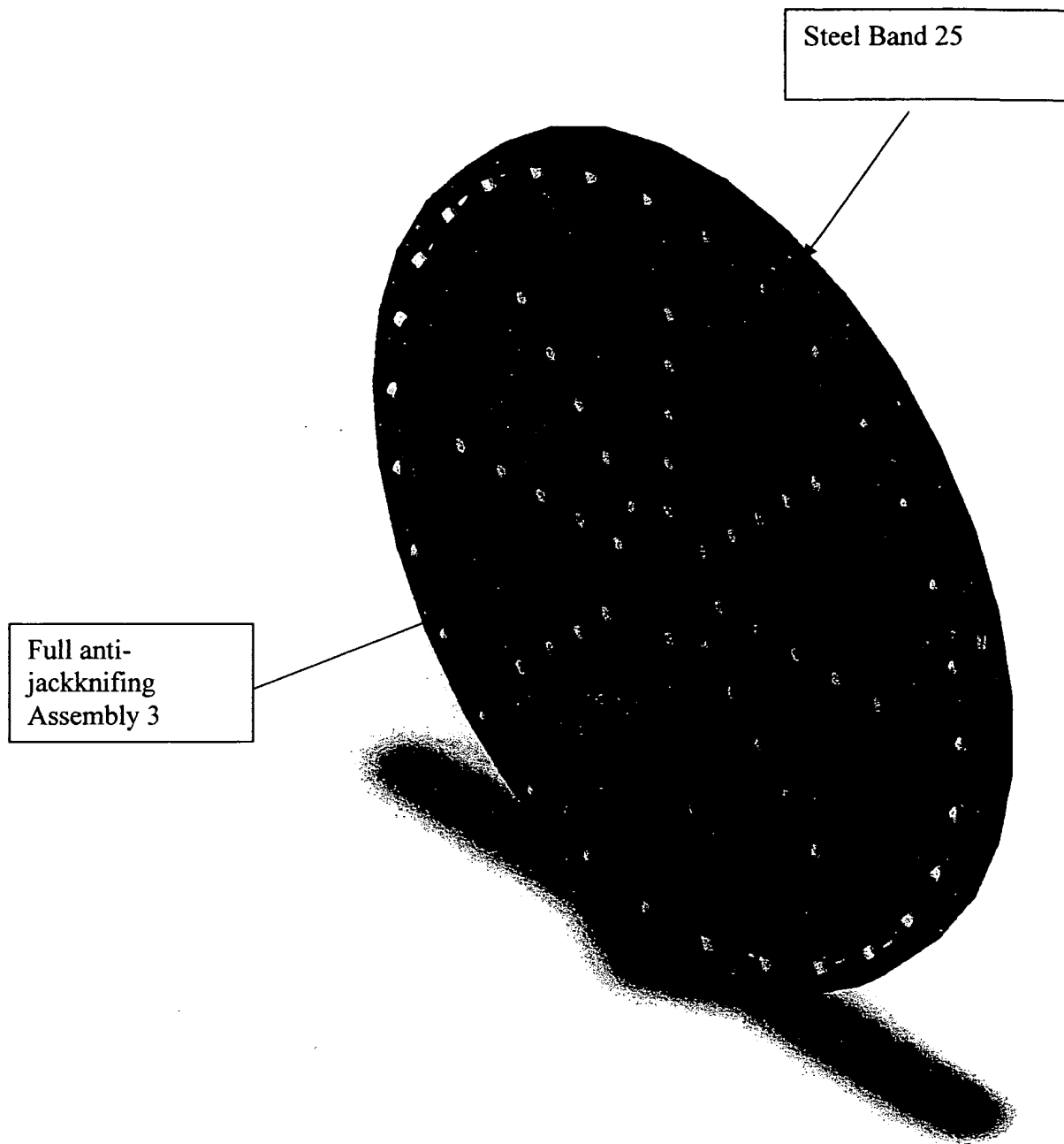


Figure 2A



Figure 3

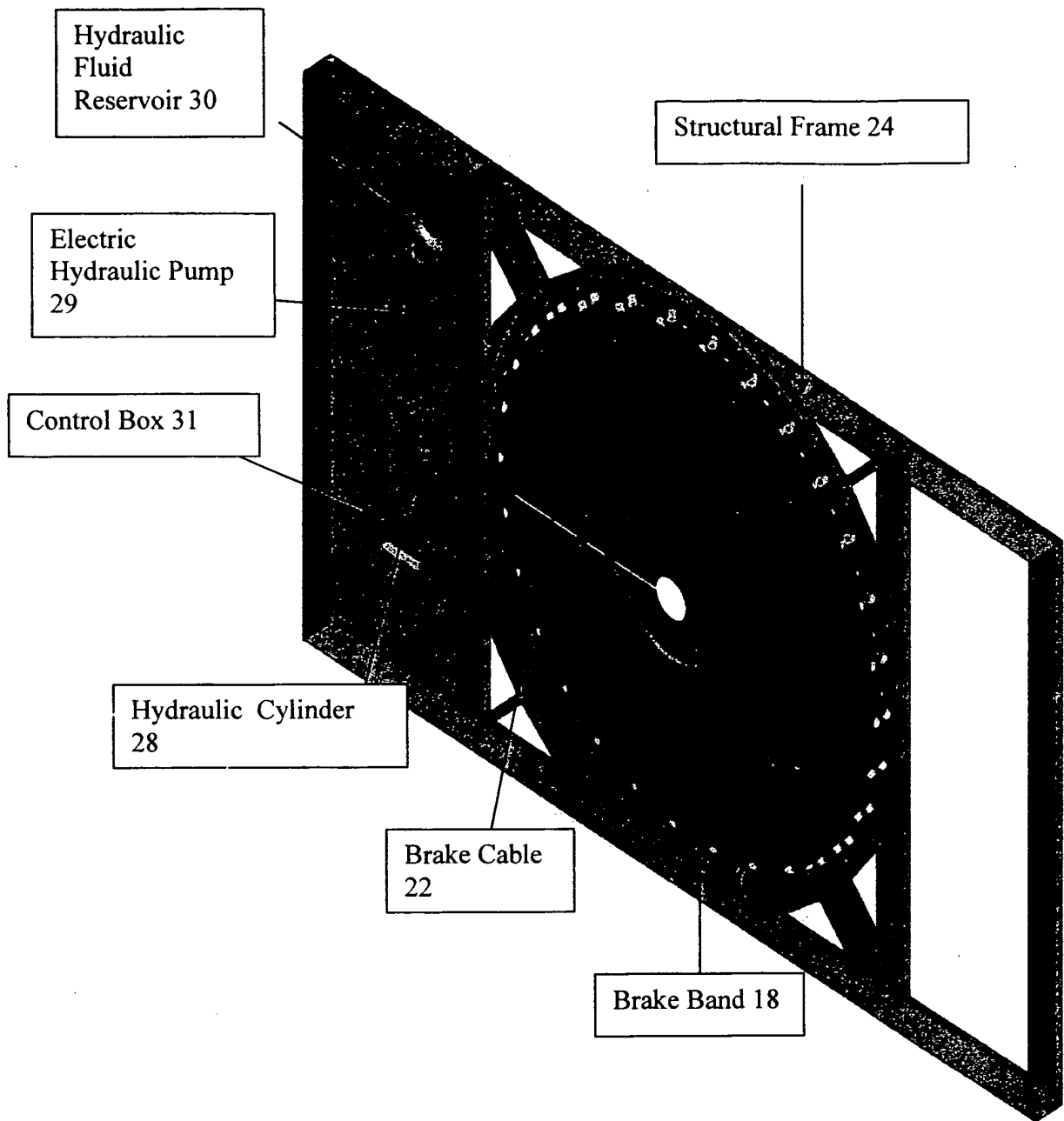


Figure 4

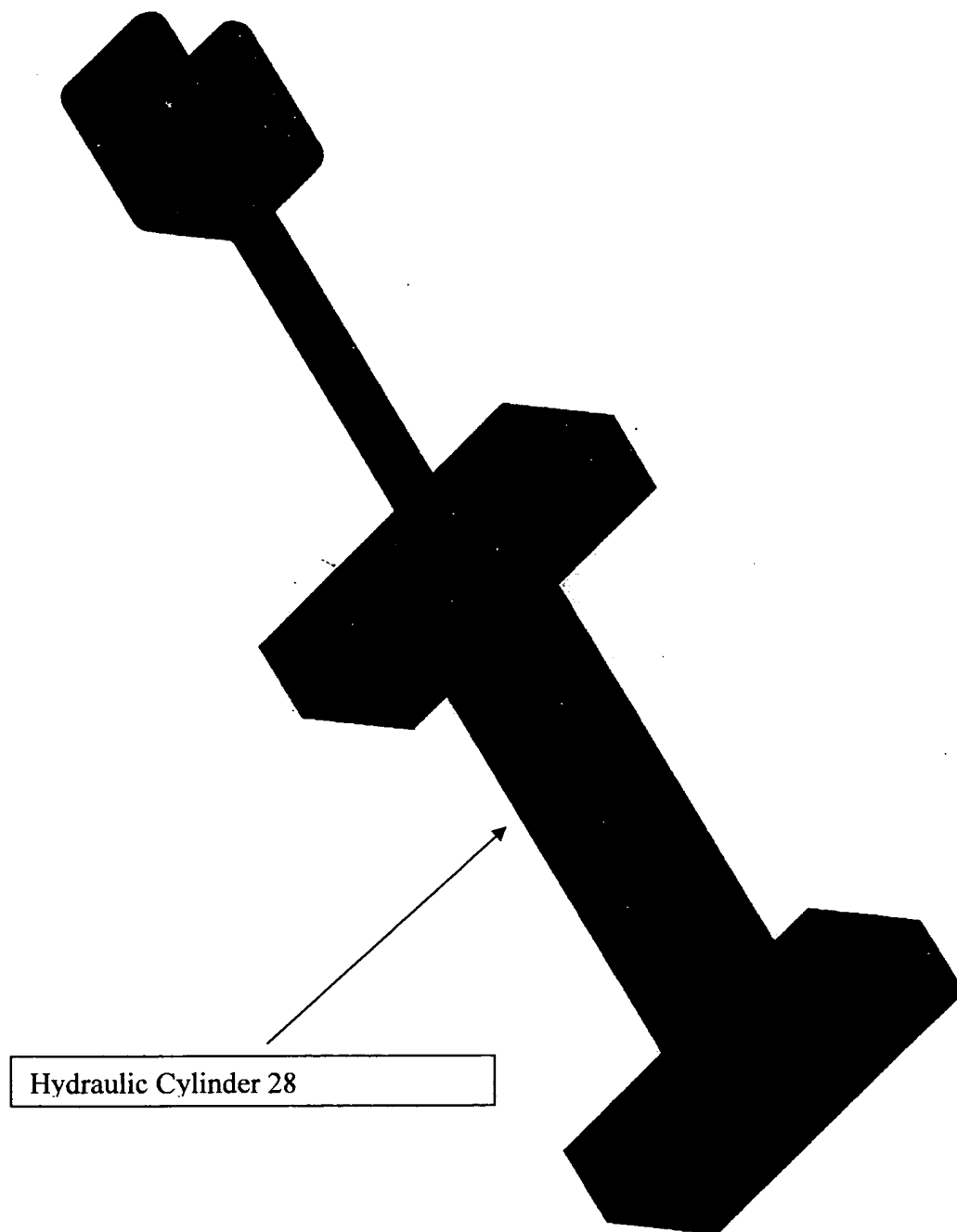


Figure 4A

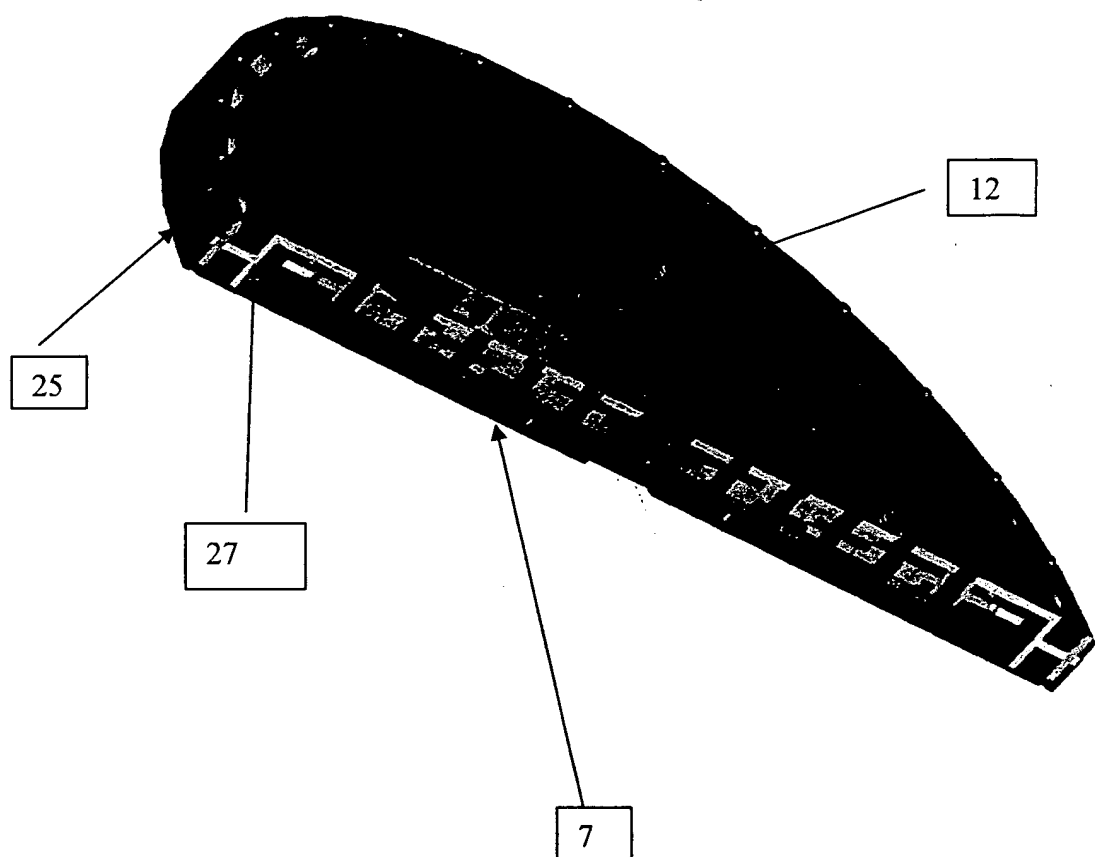


Figure 5

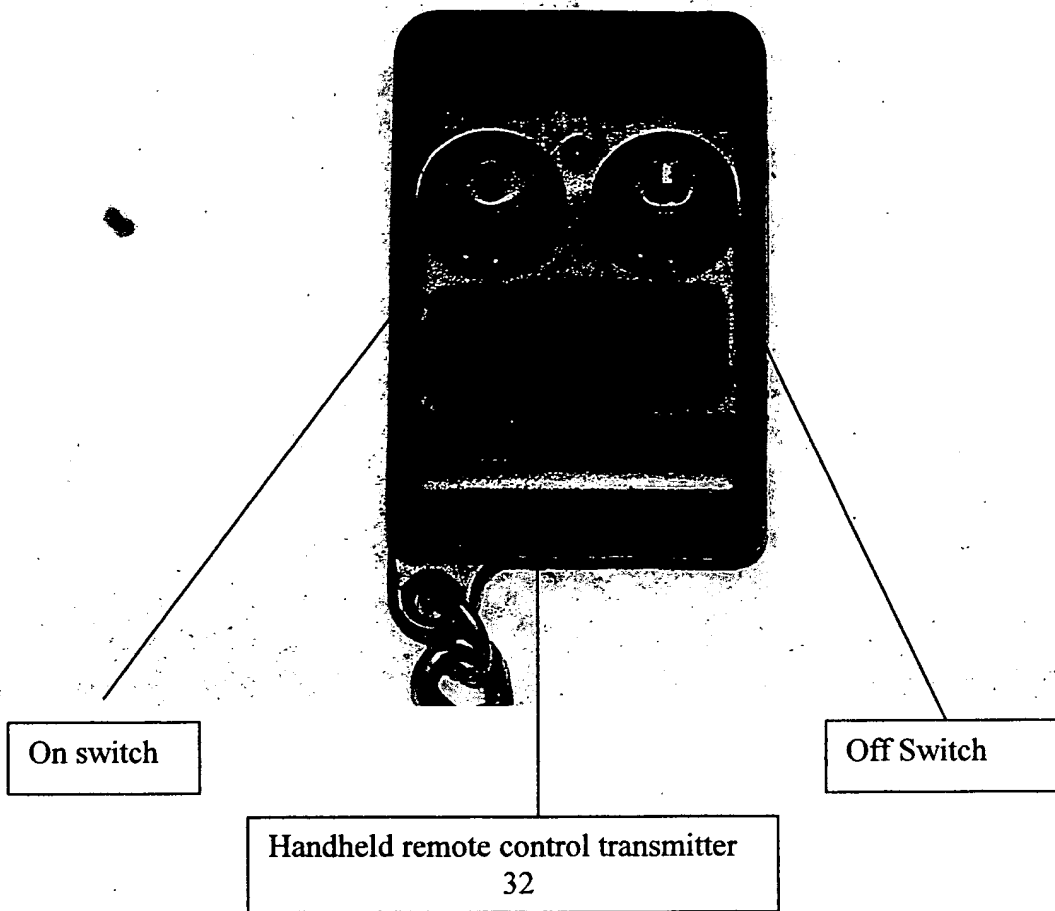


Figure 6

Logic Circuit

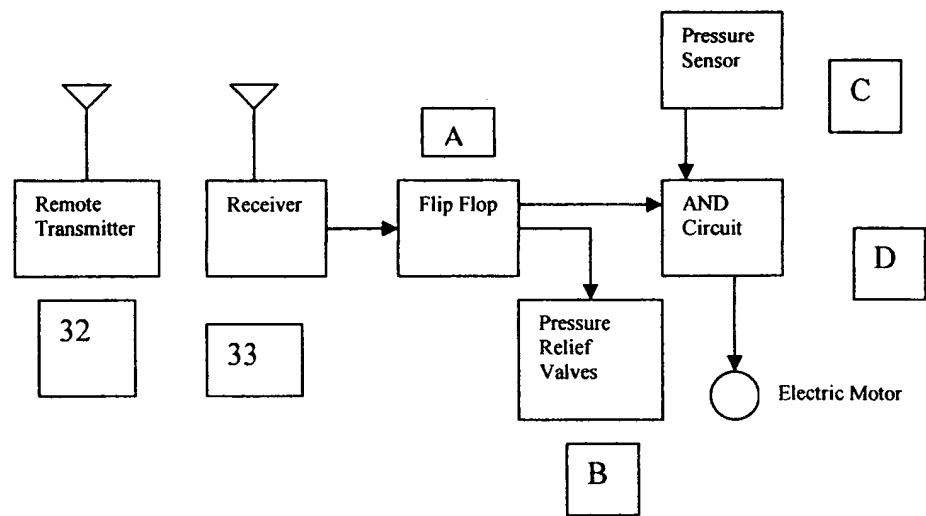
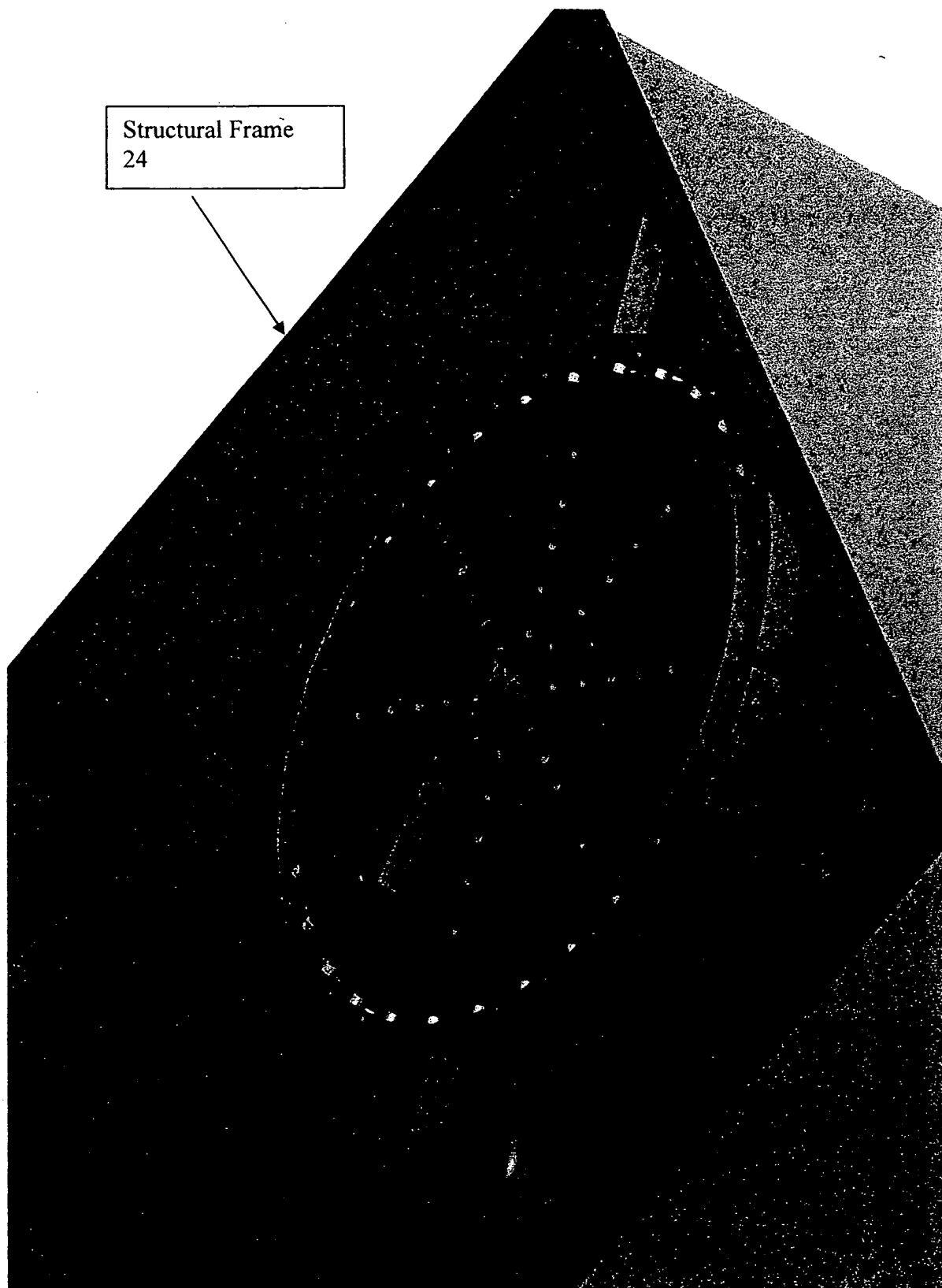


Figure 7



Structural Frame
24

Figure 7A